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Mobile Optical Pluggables Alliance (MOPA)

Technical paper on
Optical pluggable performance for tight synchronization

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1. Executive summary

The MOPA organization (https://mopa-alliance.org/) consists of RAN vendors, optical pluggable vendors and optical IC vendors. It is an industry effort publishing technical papers describing relevant high-level requirements and optical solution “Blueprints” for mobile optical transport, from the point of view of optical pluggable modules.
One of the topics considered is the ability to achieve the tight synchronization requirements for the transport of mobile fronthaul between Distributed Units (DUs) and Radio Units (RUs). In fronthaul the RUs need to be accurately time synchronized in order to support their coordination at the air interface. Depending on the category of coordination desired, the end-to-end timing accuracy between the Grand Master reference clock and each RU needs to be on the order of several tens to a hundred ns. In a packet transport network using PTP (Precision Time Protocol) for synchronization distribution, PTP timestamping inaccuracy must be tightly controlled. Any effect, deterministic or stochastic, potentially leading to uplink/downlink propagation delay asymmetry in a link, directly impacts the time error budget.

This paper reviews how optical links can impact time synchronization error (TE) in packet transport networks using Precision Time Protocol. Optical transmission links and packet processing nodes both contribute to the end-to-end TE budget, which must be compatible with the requirements of the application for which the network is providing time synchronization.

ITU-T G.8372 describes accuracy classes for nodes and incorporates in the node definition both the packet processing circuitry and the optical pluggables used on its egress and ingress ports. Anyway, it does not provide an individual TE budget for both elements.

In the past, with low (<25G) transmission bit rates, optical pluggables had a simple internal structure and their contribution to the node level budget was almost insignificant in comparison with that of the packet processing circuitry.

Since packet technologies improved a lot and optical pluggables needed to support higher bit rates, this situation changed: especially in conjunction with the adoption of DSP and complex digital parts inside the optical pluggables, capturing their contribution to the node level TE budget becomes very important.

This paper proposes a methodology to model the propagation delays across the transmit and receive signal chains of optical pluggables, breaking both down into a typical value and an uncertainty range around it.

Advertisement of the availability of Tx and Rx propagation delay typical values in certain registers of the pluggables’ EEPROM map paves the way to system-level compensation for any asymmetry between them.

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The two Tx and Rx uncertainty ranges describe the residual, non-compensable asymmetries that define the worst-case contribution of the optical pluggable to TE.

Based on this approach, a definition of accuracy classes for optical pluggables is proposed, as a fixed percentage of the node level TE budget.

This paper also suggests a possible methodology to characterize optical pluggables propagation delays during R&D Design Verification Testing, avoiding adding costly manufacturing tests, and the data structure that should be added to optical pluggables' EEPROM maps to make nodes aware of their characteristics and allow system-level compensation for the difference of the typical values.

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Contents

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2. Acronyms

5G	5th Generation mobile networks, generic term for 5G system (or just the RAN part)
5GC	5G core, packet core part of 5G system
6G	6th Generation mobile networks
AI	Artificial Intelligence
AAV	Alternative Access Vendor
APC	Angled Polished Connector
AWG	Arrayed Waveguide Grating (optical DWDM multiplexer)
BiDi	BiDirectional (using a single fiber strand for both transmission directions from an optical pluggable pair, where the two directions use different wavelengths)
BER	Bit Error Rate
C-band	The conventional fiber transmission band, around 1550 nm (aka “3rd window”)
CapEx	Capital expenditure
CD	Chromatic Dispersion
CO	Central Office
CRAN	Centralized RAN
CPRI	Common Public Radio Interface
CU	Central Unit
cTE	Constant Time Error
CWDM	Coarse WDM (20 nm wavelength spacing)
DAC	Direct Attach Copper (cable)
DCO	Digital Coherent Optics
DDM	Digital Diagnostics Monitoring
DFB	Distributed Feedback (laser)
DRAN	Distributed RAN
DVT	Design Validation Testing
DWDM	Dense WDM (<= 0.8 nm wavelength spacing in C-band)
DU	Distributed Unit
EEPROM	Electrically Erasable Programmable Read-Only Memory
FP	Fabry-Pérot (laser)
FWM	Four-Wave Mixing
HLS	High-Layer Split
HTMC	Head-to-Tail Message Channel
IL	Insertion Loss
LC	Optical Connector
LLS	Low-Layer Split
LO	Local Oscillator
LWDM	Local Area Network (LAN) WDM
MPI	Multi-Path Interference
MSA	Multi-Source Agreement
NR	New Radio, RAN part of 5G system
NRZ	Non-Return to Zero modulation

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O-band	The original fiber transmission band, around 1310 nm (aka “2nd window”)
ODN	Optical Distribution Network
ONU	Optical Network Unit (for TDM-PON)
OLT	Optical Line terminal (for TDM-PON)
OpEx	Operational expenditure
OPP	Optical Path Penalty
P2MP	Point-to-multipoint
P2P	Point-to-point
PAM4	Pulse Amplitude Modulation, 4 levels
Phy	Physical layer (optical)
Pkt	Indicates a node for packet switching and aggregation. May include mapping CPRI to packet, TDM to packet, etc.
PTP	Precision Time Protocol
QSFP	Quadruple-density Small Form Factor Pluggable
RAN	Radio Access Network
R-DDMI	Remote – Digital Diagnostics Monitoring Interface
ROSA	Receive Optical Sub-Assembly
RU	Radio Unit
SDO	Standards Development Organization
SNR	Signal to Noise Ratio
SFP	Small Form-factor Pluggable
STO	Self-Tuning Optic
TDP	Transmitter Dispersion Penalty
TDECQ	Transmitter Dispersion Eye Closure Quaternary
TOSA	Transmit Optical Sub-Assembly
UC	Use Case
VRAN	Virtual RAN
WDM	Wavelength Division Multiplexing. In a node, WDM indicates an active WDM equipment, also known as a WDM transponder
WL	WaveLength
WR	Wavelength Routed
WS	Wavelength Selected

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3. Introduction - Impact of pluggables on transported time synchronization

In a packet transport network using PTP (Precision Time Protocol [PTP]) for time synchronization distribution, PTP timestamping accuracy must be tightly controlled. Any effect, deterministic or stochastic, potentially leading to uplink/downlink propagation delay asymmetry in a link directly impacts the time error budget. The acceptable contribution of pluggables in point-to-point links to overall uplink/downlink delay asymmetry should be a small percentage of the overall requirement for the full system. For TDM-PON systems the delay is inherently asymmetric, and this is circumvented by a termination of PTP at the OLT, the use of TPS-TC (Transport Protocol Specific – Transmission Convergence), and generation of PTP at the ONU side. In the case of TDM-PON the uplink/downlink propagation delays as such are allowed to be different but they must be estimated correctly for a precise distribution of Time of Day to the ONUs.

This document reports a detailed description of node level and link level aspects of accurate sync distribution via PTP, how the characteristics of optical pluggables can impact the constant time error (cTE), and proposes a classification of optical pluggables in order to estimate and compensate for constant time errors.

3.1. Factors impacting PTP accuracy

In packet transport networks, time synchronization can be transported using **PTP** [PTP]. A time transmitter node provides high accuracy time to a time receiver node, compensating for propagation delays, via time measurements of messages including “time-stamping” in the messages (see Figure APB.1)

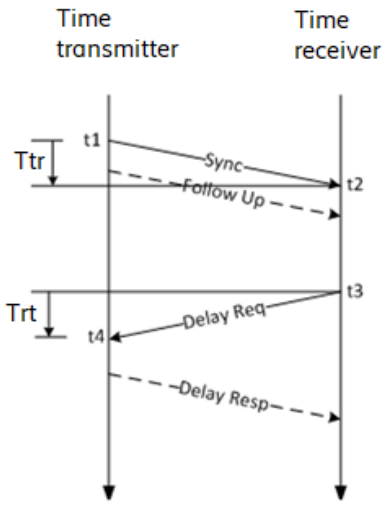

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Figure APB.1: Propagation of timing messages.

Time is calculated at the time receiver node with a very simple approach. First, the mean path delay between the two nodes is calculated based on the measured values of t1, t2, t3 and t4:

Delay = [(t2 – t1) + (t4 - t3)] / 2 = **(Ttr + Trt) / 2**

The obtained propagation delay is then used to calculate the time (clock) offset between the time transmitter and the time receiver nodes:

Offset (time transmitter to time receiver) = t2 - t1- Delay = **Ttr – Delay**

The two single-ended propagation delays, **Ttr and Trt** are assumed equal: if they are **different**, half their difference becomes a source of **time error** taken by the time receiver node.

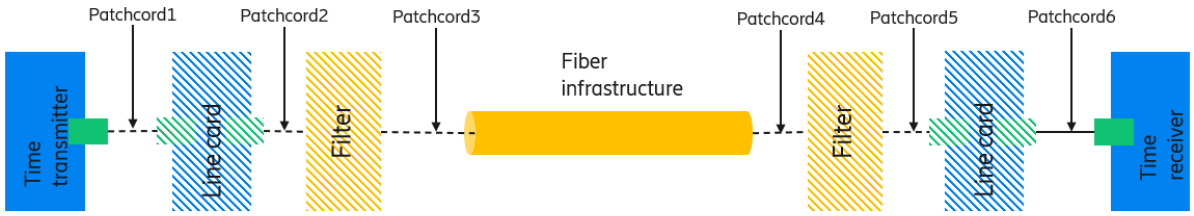

Figure APB.2: Fiber optic system with several possible delay asymmetry contributors.

In fiber optic links, there are several possible contributors to this propagation delay asymmetry (see Figure APB.2):
The most obvious one is the fibers' length mismatch, including patch-cords: considering the flight time of signals in glass fibers (approx. 5 us/km*), every meter of length mismatch contributes 5 ns of propagation delay asymmetry.* For dual fiber plants, the Tx/Rx fiber patch-cords length mismatch can be minimized using only dual fiber, "matched" patch-cords.
Concerning the outside plant fiber, due to the "loose-tube" construction technology of underground cables, in the worst case two fibers randomly picked from the same cable can exhibit a length mismatch up to 3m or 15ns, per km.
BiDi optical interfaces, initially introduced to save fiber, have become popular in the fronthaul space because they allow the removal of this contribution. This highlights a secondary effect of a dual fiber plant, i.e. the impact of fiber chromatic dispersion, causing different wavelengths to propagate at different speeds. This effect can be minimized by limiting the wavelength difference in the two directions. In estimating this contribution, wavelength drifts caused by changes in the operating

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temperature of the lasers at both ends of the links must be considered, as they may be significant in case of lasers without thermo-electric coolers ("uncooled" lasers). Anyway, this is accounted for if the worst case, over temperature and lifetime, minimum and maximum wavelengths are used for the estimation.
System internal optical and electronics components in a link can contribute to the worst-case delay asymmetry. One example is WDM optical filter fiber pigtails, which may differ in length depending on the component internal optical paths.

Lastly, optical transceivers and digital integrated circuits on the line cards can contribute to these delay asymmetry values. Standardization bodies[1] are trying to improve the timestamping accuracy process at system level, but there is no effort to put a cap on the possible contribution from optical pluggables

4. The impact of optical pluggables in link propagation delay asymmetries

For low bit rates (25 Gb/s and below), the internal structure of optical pluggables is simple and mostly "analog" in nature. The most complex electronic part in pluggables can be a simple retimer/CDR (Clock and Data Recovery). The contribution to propagation delay asymmetry of pluggables is determined by the symbol latency through optical and electrical components, and by possible length mismatches in the short PCB (Printed Circuit Board) traces, making it easy to imagine a nanosecond contribution to asymmetry even in a multi-vendor, multi-design environment.

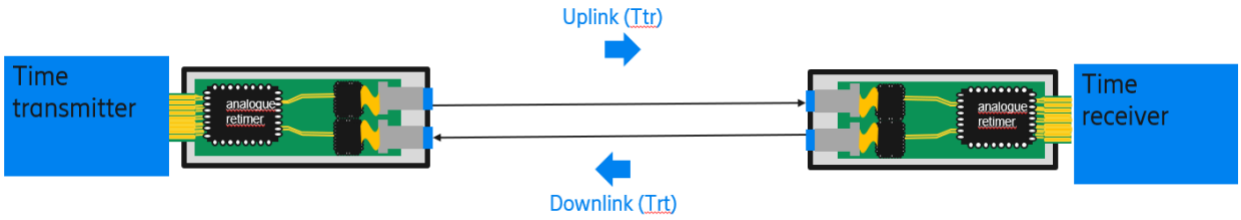

Figure APB.3: Details of a Time transmitter and Time receiver link where the optical pluggables mostly have analogue internal components.

With the rise of higher bit rates (50 Gb/s and higher) and the adoption of advanced modulation formats (PAM-4 or Coherent), complex digital signal processors (DSPs) can appear in optical pluggables. A DSP converts analogue signals into digital and implements complex signal processing functions in the digital domain. In the Tx case, it can also convert the signal back to analogue to drive the optical transmitter.

[1] *The **IEEE P802.3cx** "improving PTP timestamping accuracy" Task Force is working to make the overall timestamping mechanism more precise, especially for high-speed Ethernet aggregates partitioned over several 'stripes' or 'lanes'.*

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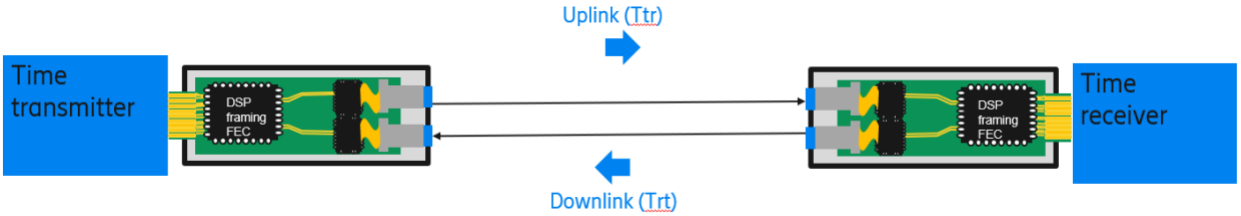

Figure APB.4: Details of a Time transmitter and Time receiver link where the optical pluggables have DSPs.

The presence of DSPs can potentially make **Ttr** and **Trt** significantly different, especially if minimizing propagation delay asymmetry was not considered as a design criterion. Different DSP vendors can have different signal pipeline architectures: but also considering a transceiver from a single vendor, with the same DSP on both ends, uplink and downlink signal paths inside the devices are nominally identical but **process/ temperature / supply voltage variations**, **DSP state machine evolution** different at both ends may introduce a propagation delay asymmetry.
In some cases, even more complex digital functions like gear-boxing, framing and FEC (Forward-Error Correction) can be implemented in the DSP and, if they were designed without the requirement to minimize delay asymmetry, they could easily dominate the contribution of optical pluggables.
System vendors, pluggable vendors and DSP vendors can *collaboratively make future DSP-based optics more "timing and sync friendly"* by characterizing and putting a cap on the propagation delay asymmetry so that the overall contribution of optical pluggables can be engineered in the complete system.

5. Views on synchronization accuracy: Per-link view, per-node view, end-to-end view

Not all networks are created equal, and different scenarios may require different tiers of PTP time accuracy. Such scenarios are described in ITU-T G.8271 and G.8271.1, and other relevant recommendations in the G.827x series. The end-to-end synchronization accuracy requirement is described in different categories of Time Alignment Errors between RUs as per 3GPP TS38.104. Such end-to-end value (in other words the synchronization TE budget) between the reference point (which can be a T-GM or a common T-BC) and the devices being synchronized is the starting point to check or design a given network deployment consisting of intermediate nodes and links. Each node and link consume part of the TE budget due to their synchronization inaccuracies. The stricter the category, the more stringent the requirement on the network elements (in terms of their amount and their performance). A worst-case approach is typically used for calculating the consumption of the end-to-end budget. As shown in figure APB.7, there are two ways to consider the break-down of the budget, namely per node or per link.

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From the point of view of a given node, its synchronization performance when acting as T-BC (Telecom Boundary Clock) or T-TSC (Telecom- Time Slave Clock) nodes in the synchronization path is described in Classes as indicated in Table 7.3 from G.8273 Annex B:

Table 7-3 – T-BC/T-TSC permissible range of constant time error

T-BC/T-TSC Class	Permissible range of constant time error – cTE(ns)
A	±50
B	±20
C	±10
D	For further study

Figure APB.5: Table 7.3 from G.8273 Annex B.

It covers the so-called “constant time error” contribution (cTE), and describes four accuracy classes, A through D, in decreasing range of permissible time error.
As an example, “Class A” nodes are normally used for mobile backhaul networks (Category C requirements) while “Class B” or “Class C” nodes may be required in fronthaul networks having to support time-sensitive features (TDD, advanced spectrum coordination in FR1 or in FR2, etc.) (Category B or Category A requirements).
“Constant” means “not varying in-service” and seems also suitable for pluggable optics: once an optical link is operational, the propagation delay asymmetry introduced by pluggables does not change significantly while a disruptive event (e.g. a fiber cut and restore or changing one of the pluggables on the endpoints to a different vendor) may cause this value to change.
ITU-T G.8273.2 defines time accuracy classes at “node” level, and the way to test time error at node level is indicated in figure APB.6:

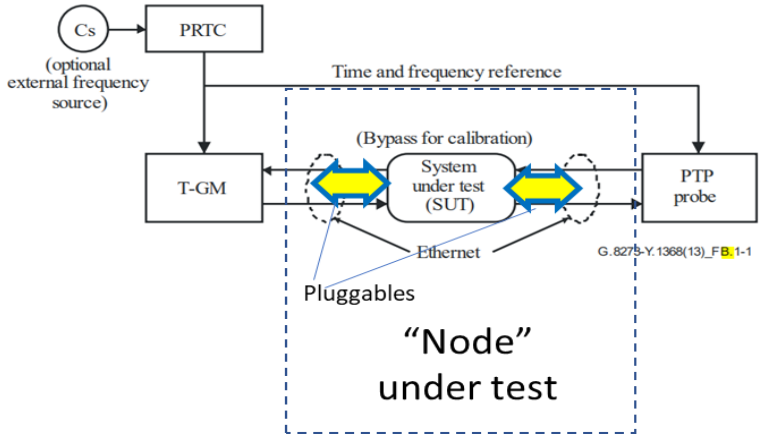

Figure APB.6: Figure B.1.1 from G.8273.2 Annex B.

Two pluggables enter in the G.8273.2 node test setup, and their Tx/Rx propagation delay differences contribute to the “node level” time error budget. If a node of a given Class is designed with a given performance excluding the pluggables, it leaves a given margin for the two pluggables. It is beneficial to be able to select appropriate pluggables based on some sort of classification.

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The other angle towards the budget is to look at individual links. Each link between two connected nodes consists of the fiber connection and the two pluggables.

The fiber propagation asymmetry can be introduced by differences in group velocity due to different wavelengths, and in the case of dual fibers by the difference in up- and downlink fiber lengths. If the fiber lengths and wavelengths are known, the asymmetry can be estimated and compensated for.

Both pluggables can show delay asymmetry between their Rx and Tx parts, and the combination of the pluggables leads to an aggregate asymmetry. If the latency values of the pluggables are known, the resulting aggregate asymmetry of the pair of pluggables can be compensated for. But unknown variations on such values leads to time errors that cannot be compensated for.

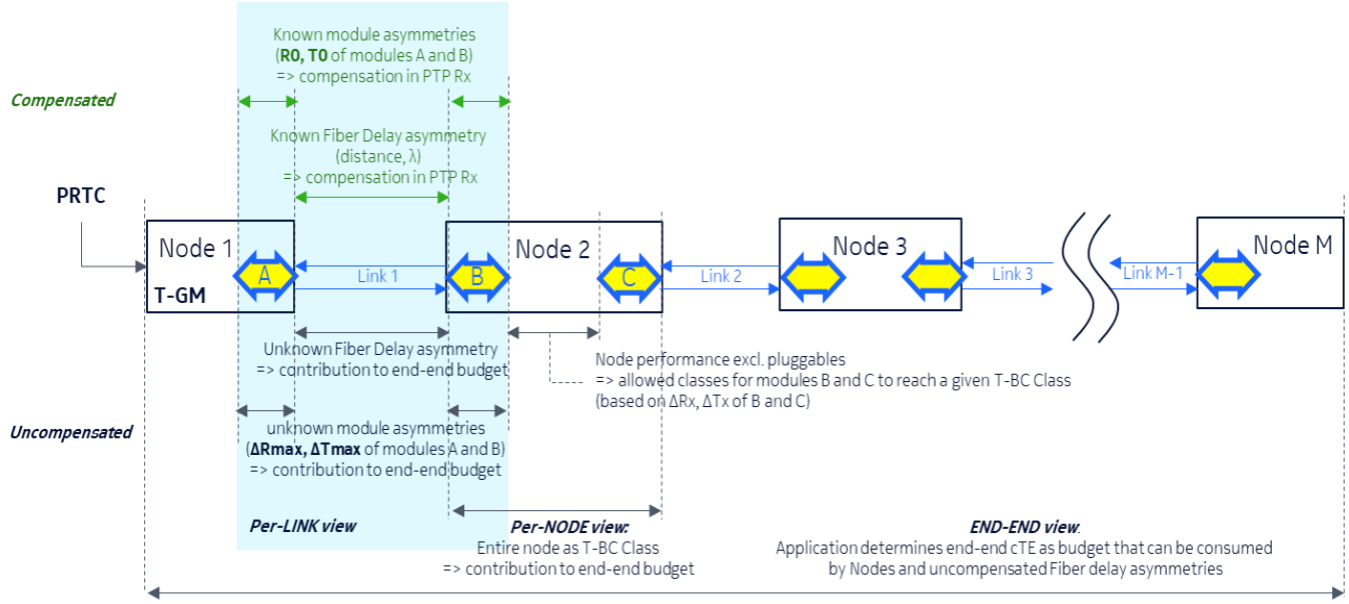

Figure APB.7: Relationship between End-to-end, per-Node, and per-link views of synchronization accuracy

It's important of course not to count the pluggables contribution twice: if considering the contribution of pluggables embedded in the "node" classification as per ITU-T, at link level only asymmetries introduced by the fiber plant and infrastructure need be considered.

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6. Eliciting transceiver-level requirements from node-level class

The assumption is that the Tx and Rx propagation delays of a transceiver "i" remain within the boundaries of a max and min value, which can be expressed as **a "typical"/average value T0 and R0 plus or minus a respective worst case (maximum) "delta" value** as shown in the diagram in figure APB.8:

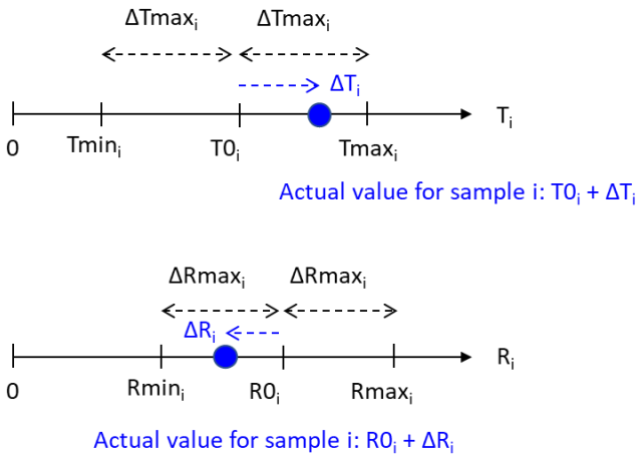

Figure APB.8: Tx and Rx average and delta propagation delay values.

These values can be measured **during Design Validation Testing (DVT)**, by grabbing a population of transceivers and measuring Tx and Rx propagation delays at corners and several times after link re-start conditions.

Considering a *couple* of transceivers "1" and "2", their **max and min propagation delays** can be written as:

$T_1 = T0_1$ +/- $\Delta Tmax_1$ $R_1 = R0_1$ +/- $\Delta Rmax_1$	$T_2 = T0_2$ +/- $\Delta Tmax_2$ $R_2 = R0_2$ +/- $\Delta Rmax_2$

"Typical"/average values may be vendor, generation and revision dependent. We could put a loose cap on them (to make sure latency is low) but variations could be accounted for by **storing these "typical" values, T0 and R0, in locations of the internal optical module EEPROM.**

Both Node A and Node B will read the "typical" values from their respective transceivers, effectively moving the *reference planes* at the fiber plant edge. The quasi-static parts (Δ) will contribute to the residual time error budget for optical pluggables. The PTP standard [PTP] describes the compensation for ingress and egress latency asymmetry in a Node. Each node A and B can perform

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the compensation individually without needing to exchange these “typical values” between the nodes.

The remaining delay asymmetry would only be dependent on the “quasi-static**”** contribution per *couple* of pluggables in a link: **$\Delta Tmax_1 + \Delta Tmax_2 + \Delta Rmax_1 + \Delta Rmax_2$** :

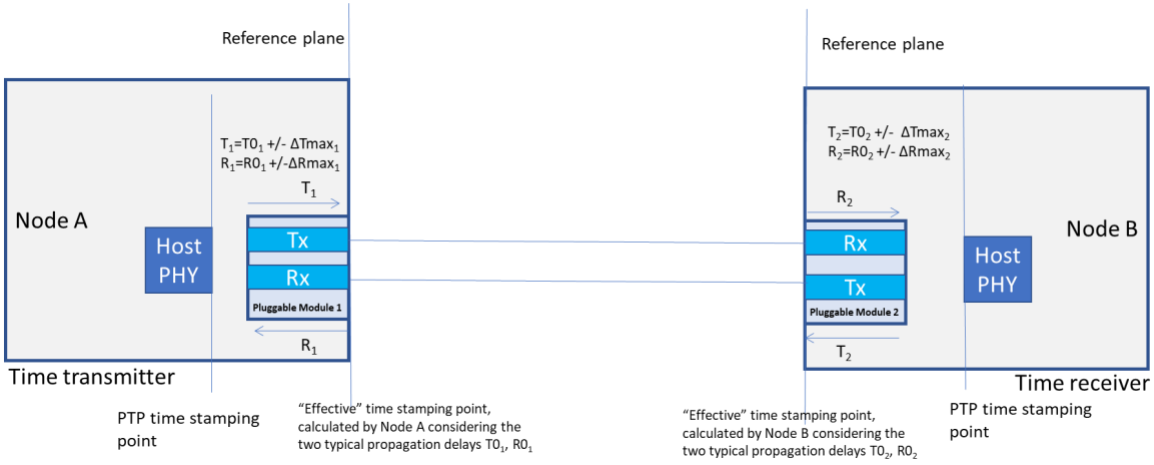

Figure APB.9: Tx and Rx average and delta propagation delay values for optical pluggables in two nodes across an optical link.

Looking now only at one side of a link - for instance, focusing on the time transmitter side:

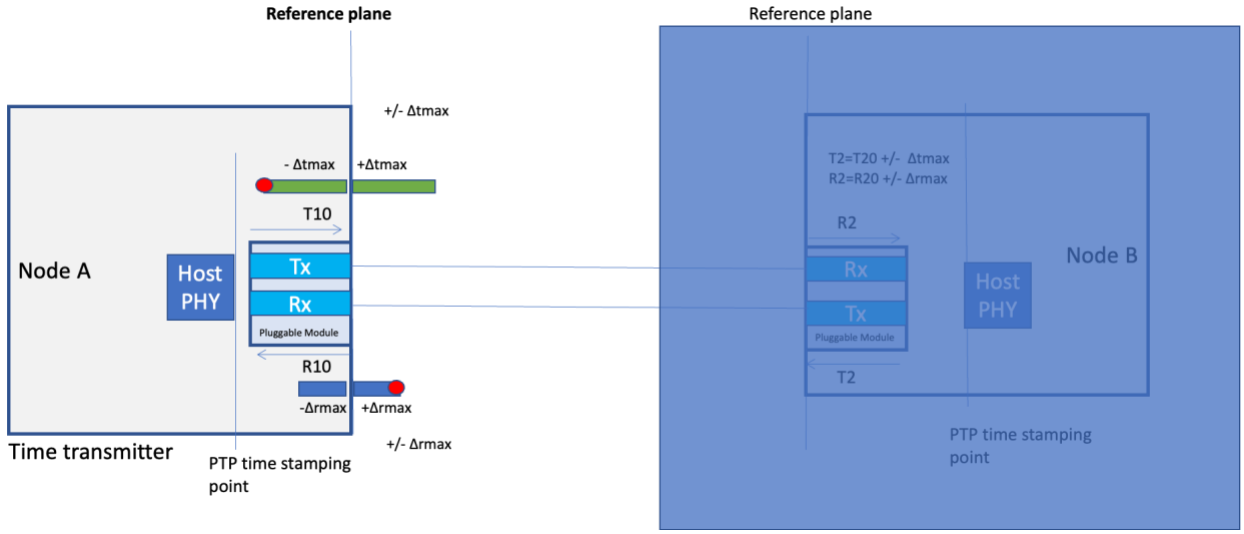

Figure APB.10: Time transmitter side average and delta propagation delay values.

Worst case error on the reference plane position happens when the two deltas on Tx and Rx are of opposite sign, so the max cTE added will simply be **½ * (ΔTmax + ΔRmax).**

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7. A methodology define propagation to delay accuracy classes of optical pluggables

Pluggable propagation delay accuracy classes can be based on “node” classes, by adding a simple percentage number.

An **“X.Y”** class pluggable would support node-level accuracy **Class X** and consume **Y%** of the relevant cTE budget (see Table APB.1 below where the G.8273.2 “node” accuracy classes are listed again for convenience). This creates a link between the node/application level and optical pluggables and defines the target optical pluggables specification.

G.8273.2 “node” accuracy classes	Class A	Class B	Class C
Max constant time error	+/50 ns	+/-20 ns	+/10 ns

Table APB.1: G.8273.2 “node” accuracy classes.

For example, a “Class C.2” pluggable consumes 2% of the cTE budget ITU-T G.8273.2 allocates for Class C nodes and hence its worst-case contribution to cTE is equal to +/-0.2ns, translating in both ΔTmax and ΔRmax = +/-0.2 ns. Such target values appear achievable for very simple pluggable implementations, maintaining an analogue signal chain.

A ”Class A.20” pluggable instead consumes 20% of the cTE budget ITU-T G.8273.2 allocates for Class A nodes and hence its worst-case contribution to cTE is equal to +/-10ns, translating in both ΔTmax and ΔRmax = +/-10 ns. These target values should enable use of quite complex digital parts inside the pluggable,

In table APB.2 we propose a meaningful definition of pluggable transceiver classes, in decreasing order of worst case cTE contribution:

	Class A.10	***Class A.20***	***Class B.10***	***Class B.20***	***Class C.2***	***Class C.10***
Max constant time error budget allocated to one pluggable	*+/- 5 ns*	*+/-10 ns*	*+/- 2 ns*	*+/- 4 ns*	*+/- 0.2 ns*	*+/- 1 ns*
	ΔTmax=+/-5ns	*ΔTmax=+/-10ns*	*ΔTmax=+/-2ns*	*ΔTmax=+/-5ns*	*ΔTmax=+/-0.2ns*	*ΔTmax=+/-1ns*
	Δmax=+/-5ns	*Δrmax=+/-10ns*	*Δrmax=+/-2ns*	*Δrmax=+/-5ns*	*Δrmax=+/-0.2ns*	*Δrmax=+/-1ns*

Table APB.2: Proposed optical pluggable classes.

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While such pluggable transceiver accuracy classes are related to node classes, it doesn't mean a class C.x transceiver can only be used in class C nodes. What's important is the intended maximum constant time error contribution of pluggables, to be used in node and link level cTE budgeting. Using more accurate pluggables in a less accurate node class (e.g. Class C.x pluggables in a Class B node) is always possible, and relaxes cTE requirements for the rest of the node. Using less accurate pluggables in a more accurate node class (e.g. Class A.x pluggables in a Class B node) may still be possible if the overall node level cTE budget is still met. It is also allowed for both ends of a link, or both ports of a node, to use pluggables of different classes as long as the end-to-end cTE budget is still met.
It is important to note that for cost reasons, the accuracy class to which a certain pluggable belongs should be guaranteed by design, and compliance to the specs should be ensured during DVT, not during manufacturing verification tests.
For pluggables supporting **multiple bit rates**, the exact configuration of the Tx/Rx signal chain may depend on the bit rate setting. If different operating modes bring significant differences in Tx and Rx propagation delay, all operating modes should be characterized. Different modes might support different accuracy classes and could have different "static" delay values, which should all be represented in the internal EEPROM.

7.1. Structure of the additional EEPROM data content for propagation delay characterization

The data structure in the optical transceiver EEPROM is expected to support the data necessary to estimate propagation delay contributions of the pluggable module and to apply propagation delay compensations for the module.

The data structure needs to take two realities into account.

Firstly, some pluggable modules use multiple parallel electrical data interfaces (lanes) to the host, and internally convert the electrical lanes into a (same or lower) number of optical channels. As the ethernet frames are distributed over the different lanes in blocks of multiple bytes, the bytes in the PTP message used for time measurement could travel across any of the lanes. Different lanes can have different Rx / Tx latencies. An accurate compensation of delay asymmetry requires the selection of the appropriate lane latencies (their T0, R0).
According to IEEE 802.3cx-2023, the transmit host must use a reference plane for the timestamping at midpoint between the slowest and the fastest lane, and the receiving host must equalize the skew of the individual lanes and use a reference plane for the measurement on the lane with lowest deskew. Both actions can be performed when the host knows the static T0 and R0 values for each individual electrical lane.
Note that additionally the host can have a single TimeSync client per module, or multiple TimeSync clients per module. Each client needs knowledge of its "own" module latency values. This is covered by having access to the static values of every electrical lane.

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Some examples of modules having 4 electrical lanes and requiring 4 sets of typical latency values R0, T0;

- 100GBASE-SR4 with CAUI-4 (break-out mode to 4 x 25GBASE-SR): module is used by 4 TimeSync clients on the host and consists of 4 electrical lanes into 4 optical channels over 4 separate fibers.
- 100GBASE-LR4 with CAUI-4: module is used by single TimeSync client on the host and consists of 4 electrical lanes into 4 optical channels (wavelengths) over a single fiber.
- 100GBASE-DR4 with CAUI-4: module is used by single TimeSync client on the host and consists of 4 electrical lanes into a single optical channel.

Regarding the quasi-static values ΔTmax and ΔRmax, a module is only as precise as its “weakest” lane. Hence only a maximum value of ΔTmax and of ΔRmax across all lanes is necessary for the classification of the module.

Secondly, modules with multiple modes of operation (e.g. multiple bitrates) are expected to allow the host to read the appropriate R0, T0 latency values for each mode as they can vary between the modes. To allow for difference in classes between modes, also the ΔTmax and ΔRmax values must be available per mode.
However this does not mean that all modes need to be readable by the host at the same time, it is actually less error-prone to have a single host-readable memory range for the module, and having the module internally update the values of that range based on the current mode of operation. In this way the host does not need to interpret mode “labels” and to correlate them with the current mode.

Therefore, the proposed content of the data structure consists of:

- Number of modes the pluggable module supports.
- Number of electrical lanes in the module.
- Per lane (updated by the module for its current mode):
  Typical Tx propagation delay (T0), Typical Rx propagation delay (R0).
  - the suggested range is at least 10 ps to 50 μs.
  - The minimal format is Q16.8 (unsigned Q format [Q format]: 0 to 2^16-2^-8) in ns units (larger formats are possible as well).

- ·Maximum over all lanes (updated by the host for its current mode):
  quasi-static Tx propagation delay (ΔTmax), quasi-static Rx propagation delay (ΔRmax).
  - the suggested range is at least 10 ps to 100 ns.
  - The minimal format is Q8.8 (in ns units) is sufficient (unsigned Q format: 0 to 2^8-2^-8). (larger formats are possible as well).

The latency class of the pluggable module (in a given mode) is deduced from the maximum of its ΔTmax and ΔRmax values.

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In terms of standardization, MOPA's goal is to define a solution that serves as future-proof basis for different pluggable types, covering single lane, multiple lanes, single operational mode, and multiple operational mode modules. A first step is the specification and inclusion of the above-mentioned parameters in SFF 8472 which covers single-lane single operational mode SFPs. This specification already contains a dedicated memory page for time-related parameters, mainly focused on extremely demanding scientific applications. The current definitions have a partial overlap with the Tight Sync parameters defined in this paper. This memory page can be updated to take both use cases into account (scientific and general communications) and adopt a structure that allows for multiple lanes in other specifications (e.g. SFF 8636 for QSFP, OIF CMIS for modules with more than 4 lanes). This is an on-going effort.

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7.2. Pluggables propagation delay characterization principles

While it is important to have numbers for propagation delays that can be used for cTE budgeting, it is equally important that the determination of such numbers is not a cost adder for the pluggables. We do not anticipate individual transceiver characterization during volume manufacturing tests will be necessary. The proposed approach to modeling propagation delays should enable a *guaranteed by design* approach, supported by characterization of a statistically significant population of individuals exposed to a variety of corner conditions during the DVT phase.

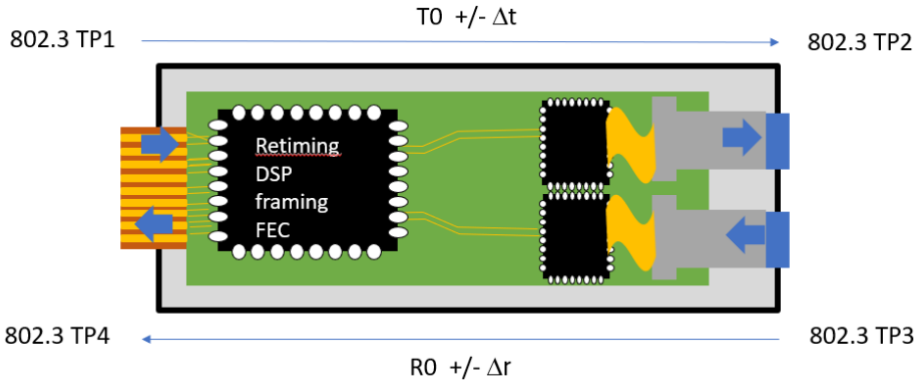

Figure APB.11: measurement points.

Propagation delay in Tx will be measured between the electrical pluggable input and the optical Tx connector output, using the nomenclature of IEEE 802.3, between test points TP1 and TP2. Propagation delay in Rx will be measured between the optical Rx connector input and the electrical pluggable output using the nomenclature of IEEE 802.3, between test points TP3 and TP4. Repeating these basic measurements over a significant number of units, exposed to corner combinations in terms of voltage, case temperature, unit's soft and hard restarts, fiber connection/disconnection events, it will be possible to create distribution histograms of the measured values.

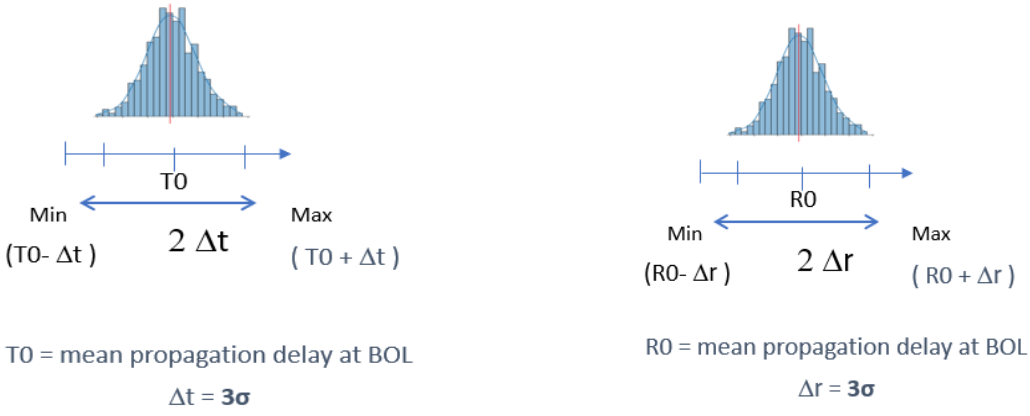

Figure APB.12: Histogram measurements

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The “typical” propagation delays for Tx and Rx will be the mean values of both distributions. The “quasi static” part will be set at three standard deviations from the mean value. These four values for each supported bit rate, determined during DVT, will then be written in the internal EEPROM map of all the individual transceivers belonging to that design generation, as described in 6.1.

7.3. Propagation delay measurement principles

Propagation delay measurement of pluggable optical modules during DVT activities should be simple, and it should be possible to execute them with test equipment and standard hardware commonly found in pluggable module design labs, such as pulse pattern generators, sampling oscilloscopes and evaluation boards.

As in all measurement methodologies, attention must be paid to achieve a measurement uncertainty at least one order of magnitude better than the values to be measured.

This can be particularly challenging for the most stringent module classes, where Tx and Rx propagation delays to be measured can be in the order of tens of ps. In this case, to achieve the needed measurement accuracy, extra care must be taken in de-embedding all the possible propagation delay contributions not caused by the device under test (DUT): PCB traces, RF cables, optical patch-cords, etc.

7.3.1. Example of a Tx path propagation delay measurement sequence

All elements on the signal path should be characterized: for instance, the propagation delay of optical patch-cords can be measured with a simple pulse pattern generator (PPG) and digital communication analyzer (DCA) oscilloscope measurement. NRZ is used in the example, but it’s possible to execute the measurement on PAM-4 signals using more complex trigger sequences instead of triggering on single bits. For instance, it’s possible to characterize the propagation delay of a patch-cord:

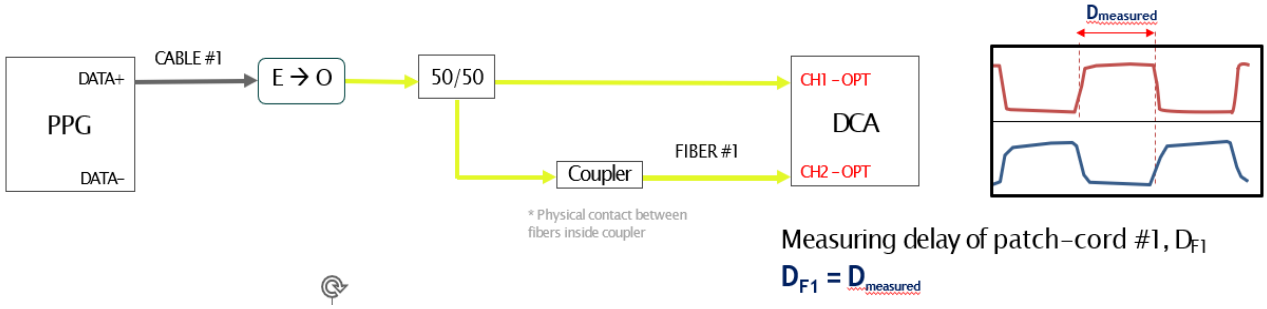

Figure APB.13: Measurement set-up for propagation delay of an optical patch-cord.

The characterized patch-cord can then be used in the Tx propagation delay measurement chain in the picture.

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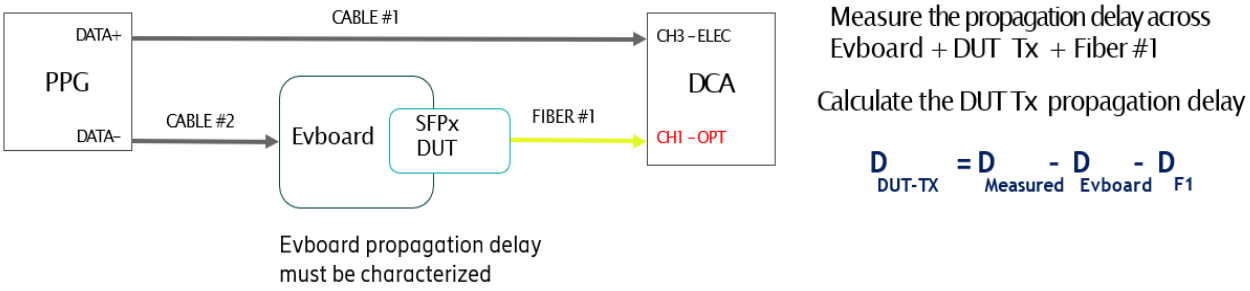

Figure APB.14: Measurement set-up for Tx propagation delay.

Similarly, when measuring the propagation delay for the Rx path, it may be necessary to use electrical cables with a known propagation delay, that can be used in the measurement setup:

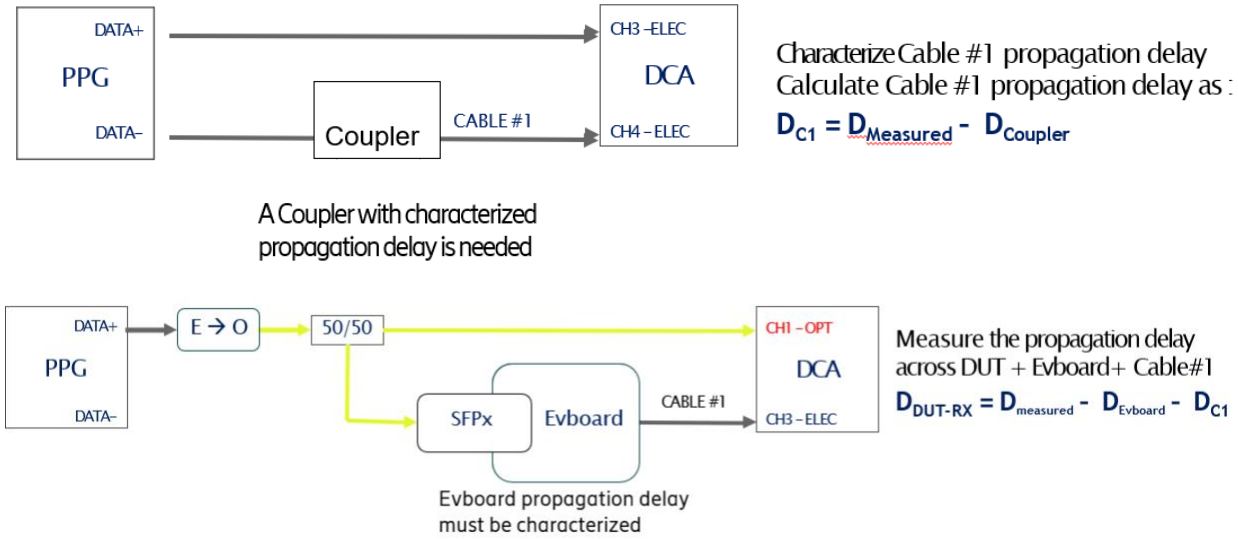

Figure APB.15: Measurement set-up for Measurement set-up for Tx propagation delay (bottom) using electrical cables of known propagation delay (top).

In both cases, it is very important to use a pluggable transceiver evaluation board with known (pre-characterized) propagation delays in Tx and Rx, and couples of phase-matched electrical cables and length-equalized optical patch-cords (or, as an alternative, the corresponding skews can be pre-characterized in and de-embedded from the final measurement).

Characteristics of test equipment (analog bandwidth, stability of time bases, etc.) must be adequate to the specific measurement needs, their detailed definition is beyond the scope of this paper.

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It must be noted that, if the pluggable integrates electronic integrated circuits requiring a specific frame format to operate, the PPG must be able to reproduce a certain number of valid frames to provide a suitable stimulus to the device.

The specific case of coherent optical transceivers is for further study, but if for example it is possible to say that the contribution of the coherent ASIC dominates the propagation delay at whole pluggable level, then the task to characterize worst case propagation delays could be delegated to ASIC and the pluggable might simply report such values in the EEPROM data.

8. An example of link cTE budgeting

Pluggables are just a part of a node/link, and the overall cTE at system level also depends on the optical infrastructure and the hosts. Therefore, it may be possible to meet the intended cTE limit for a given application *with different allocations of cTE to the different contributors*.
The following figure illustrates the different contributions of a given link between two nodes to the end-end cTE. Nodes A and B have a link composed of module i on Node A, module j on Node B, and interconnecting fiber. (For completeness, the contributions to cTE can also be considered at Node level as shown at the bottom of the figure).

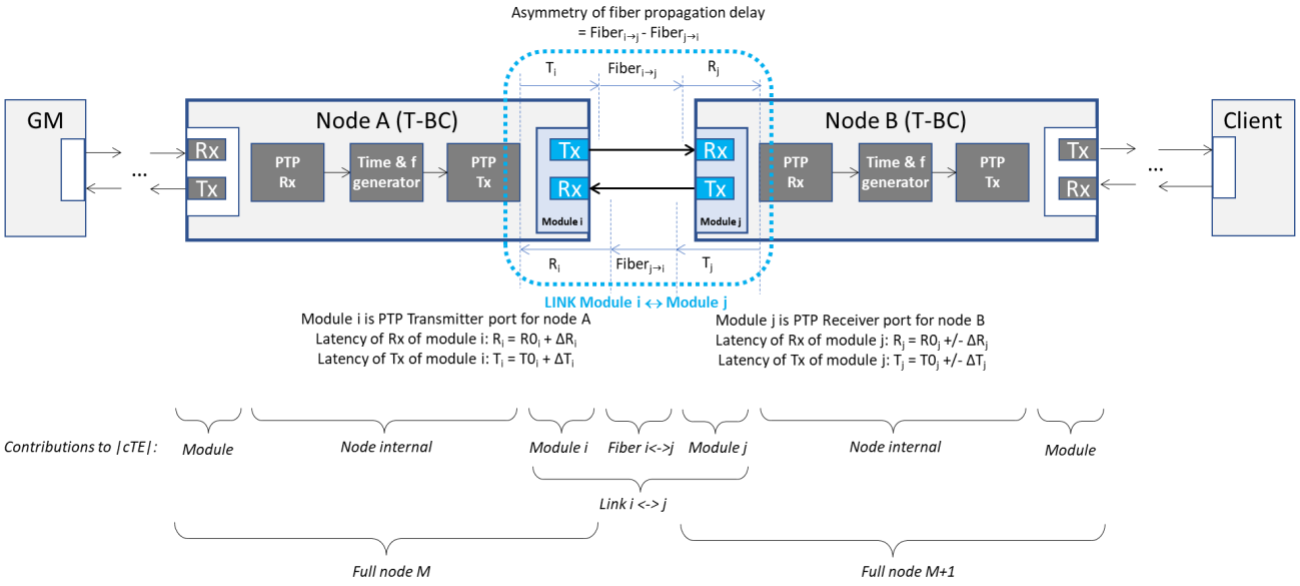

Figure APB.16: Different propagation delay contributions to end-to-end cTE.

The typical values R0, T0 of both modules are known and can be compensated for in their respective PTP functions, as described in IEEE 1588 [PTP]. In case the optical interconnection between i and j is also known (fiber distance, fiber type, wavelengths used by the Tx of modules i and j) the fiber propagation asymmetry can be deduced and can also be compensated for at the PTP receiver side. The compensated values t1', t2', t3', t4' are then used in the PTP process.

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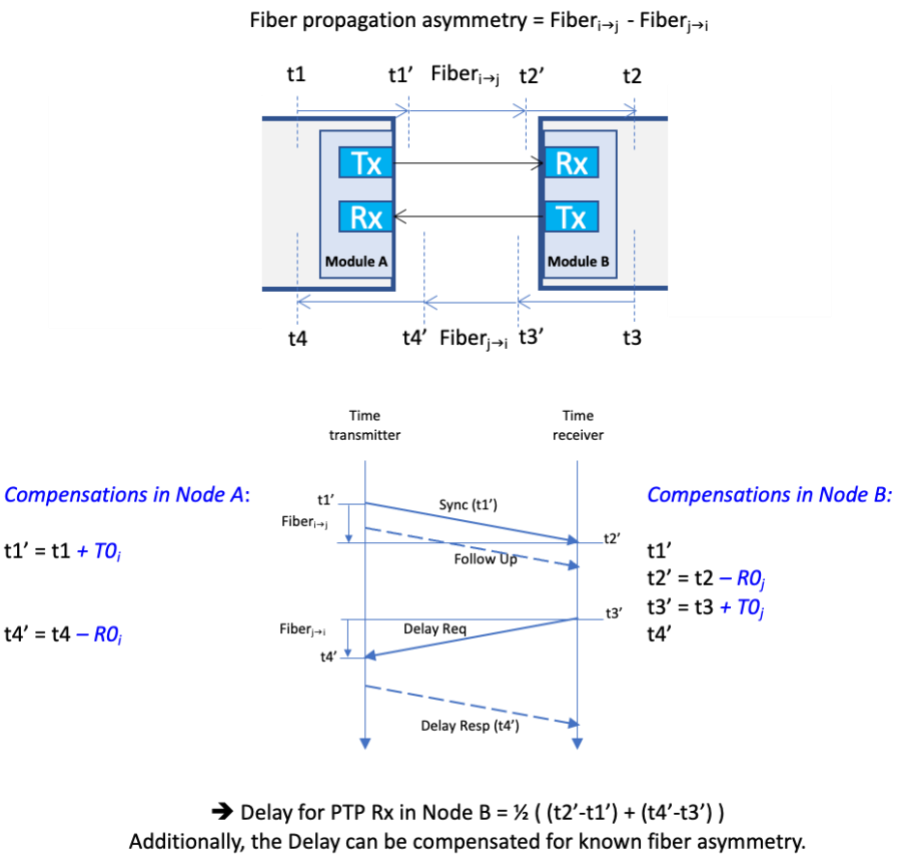

Figure APB.17: Propagation delay compensation in nodes across a link.

The remaining contribution to cTE of the link i<->j is composed of the unknown (and hence uncompensated) asymmetries of modules i and j, and the fiber propagation in case the optical interconnection is not known (e.g. unknown fiber distance):

± ½ [max asymmetry$_i$ + max asymmetry$_j$ (+ max asymmetry$_{fiber}$ if unknown)]

With the module asymmetries determined by their respective Class;
Module i Class => **max asymmetry$_i$ = ΔTmax$_i$ + ΔRmax$_i$**
Module j Class => **max asymmetry$_j$ = ΔTmax$_j$ + ΔRmax$_j$**

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9. Classes for TDM-PON optics

For **TDM-PON OLT and ONU pluggables** the asymmetry in up- and down-stream directions is allowed. The ranging process for basic ONU operation takes the round-trip delay into account. But unknown contributions to cTE in each direction must be limited to reduce the inaccuracy of the ToD deduction in the ONU. A similar classification as above can be taken for TDM-PON pluggables. Note that PON systems are modeled as a pair of media converters in G.8271.1. The whole PON system includes OLT uplink optics, OLT node, OLT PON optics, Optical Distribution Network (ODN), ONU PON optics, ONU node, and ONU UNI optics.
For consistency the contribution to cTE by the OLT PON optics and ONU PON optics (together with the ODN forming a PON link) can follow the same classification designation as for point-point optics.

10. References

[PTP] IEEE 1588-2019 “IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems”, 2020-06-16
[Q format] See https://en.wikipedia.org/wiki/Q_(number_format)