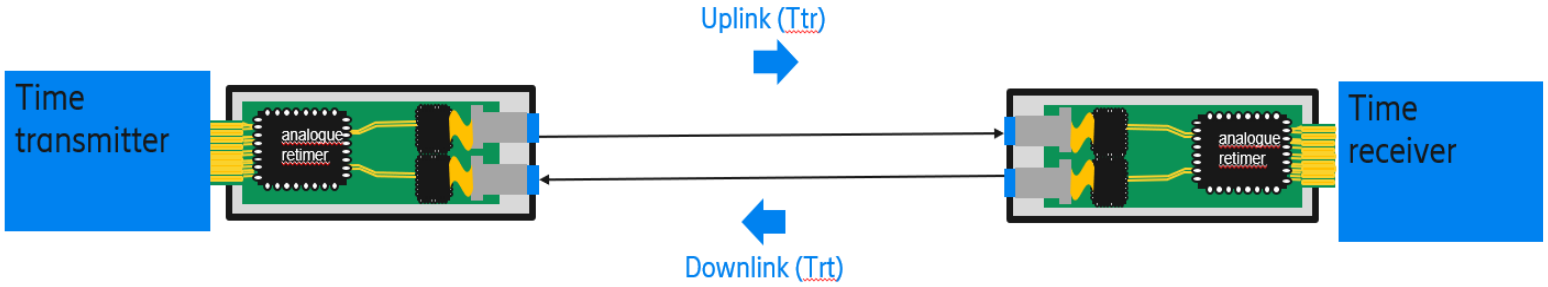
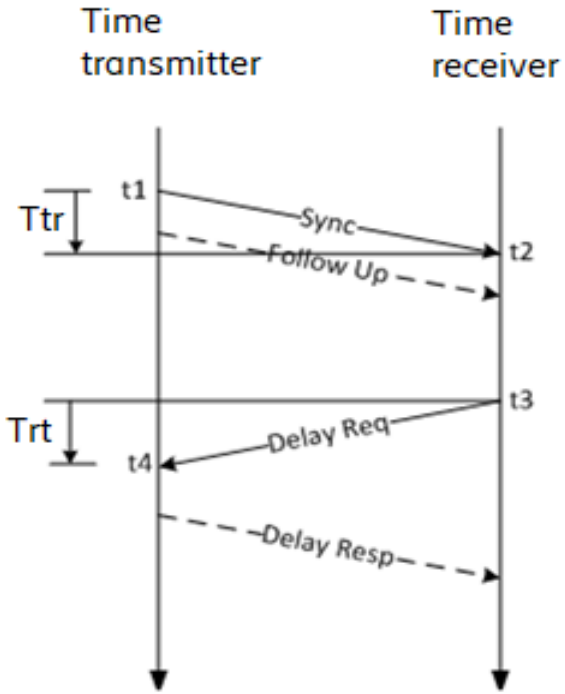
MOPA
Mobile Optical Pluggables Alliance

Appendix B: pluggables and "tight sync"

Antonio Tartaglia
François Fredricx

Precise time protocol (IEEE1588)



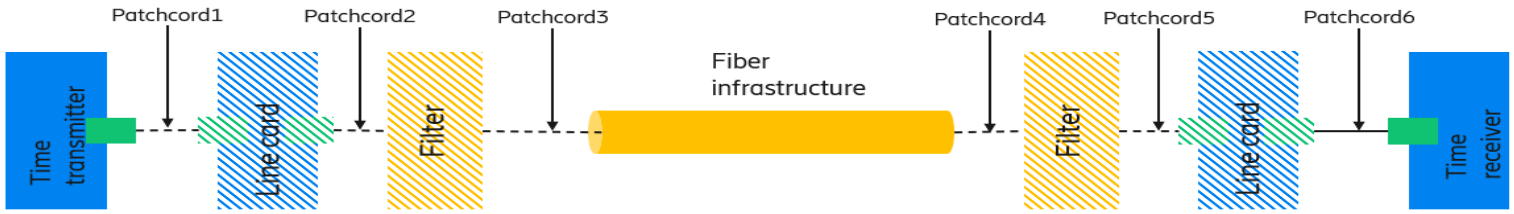


Delay = [(t2 – t1) + (t4 - t3)] / 2 = **(Ttr + Trt) / 2**

Offset = t2 - t1- Delay = **Ttr – Delay**

*If Ttr and Trt are different, half the difference becomes **time synchronization error** for the time receiver*

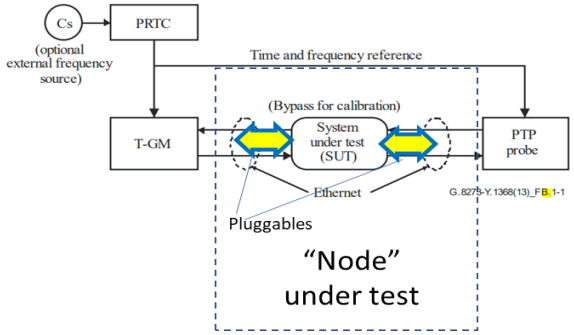
Links, nodes and networks

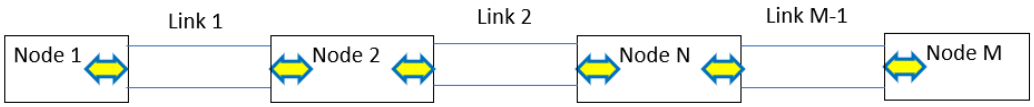


Link level view: all the uplink/downlink propagation delay asymmetries are considered, *except for pluggable optics*

Node level view:
ITU-T G.8273.x define several “classes” of time synchronization error for nodes. *Pluggable optics contribution* is included in the overall time synchronization error of the *node* using it

Network level view:
A network is made of nodes connected by links, the acceptable overall time synchronization error depends on the application

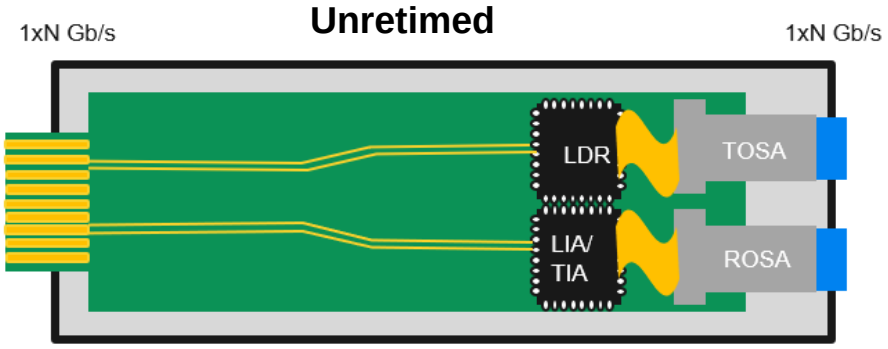




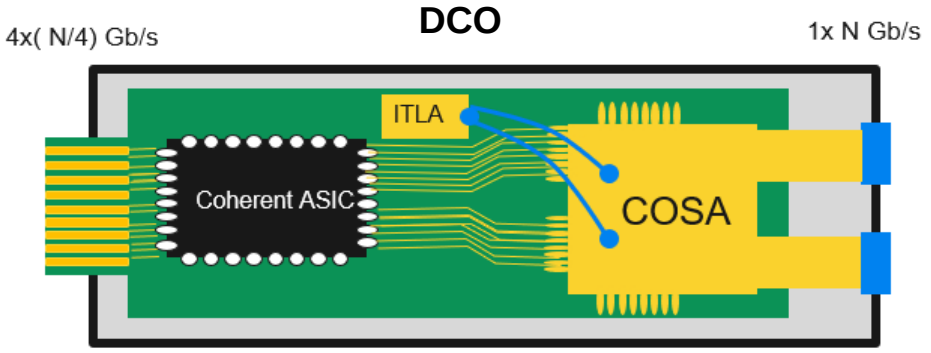
Complexity of pluggables has been increasing with the bit rate

Complex digital parts in pluggables are a potential source of constant time error (cTE)

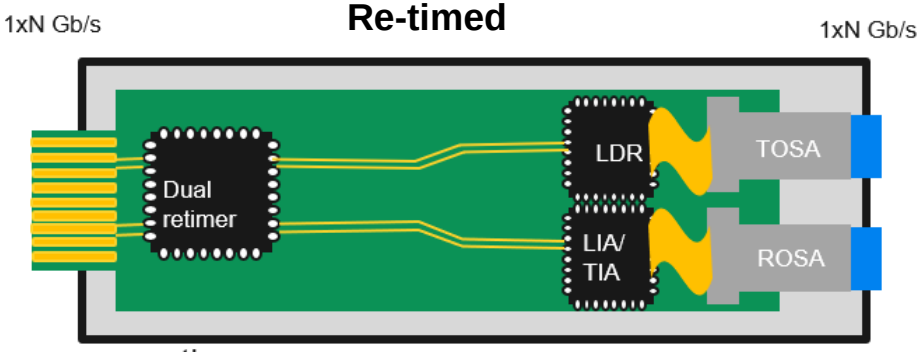
Unretimed



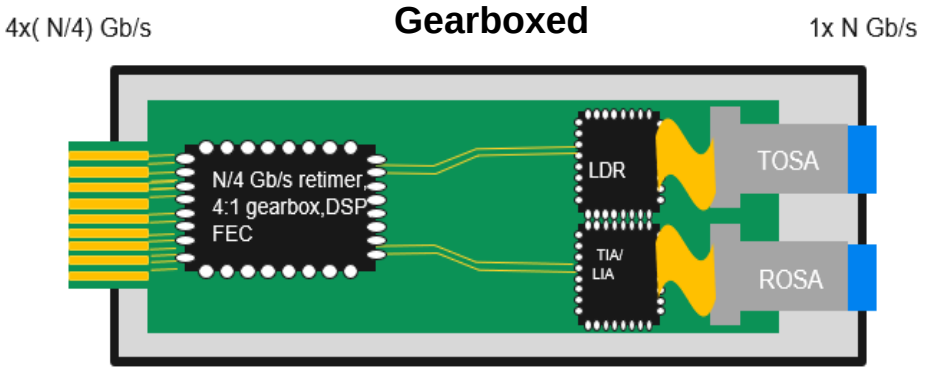
DCO



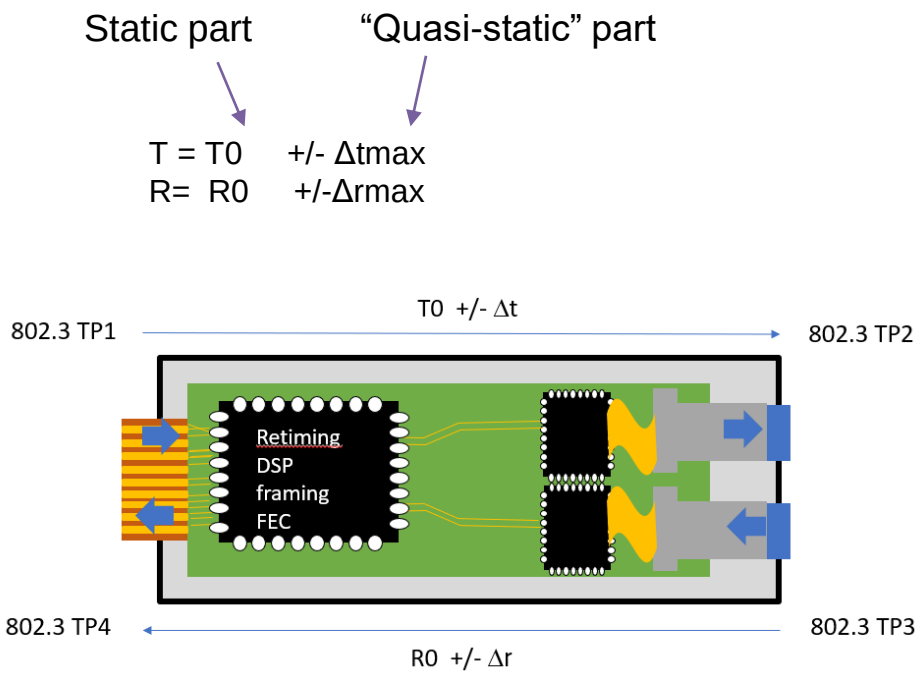
Re-timed

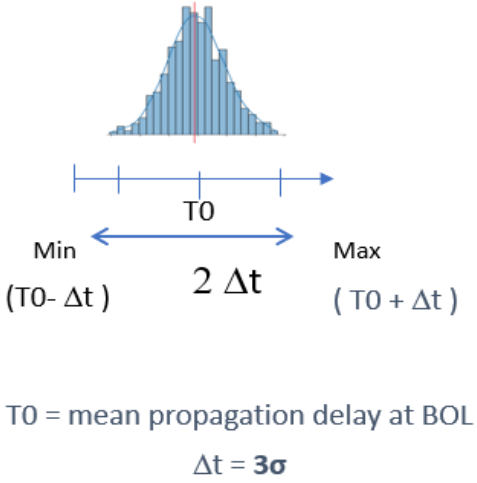


Gearboxed



Transceiver propagation delays model and DVT measurements





T0, R0 stored in transceiver’s EEPROM and **compensated for at node level.** Only Δtmax and Δrmax contribute to the worst case cTE, which for a **single** pluggable is

cTE max = +/- ½ (Δtmax + Δrmax)

Limits on cTE max for pluggables can be defined as a *percentage* of the overall cTE budget for the node in which it is used

Class C.2 pluggables → consuming 2% of the cTE budget of a Class C node

What's new in MOPA2.1

Six pluggable accuracy classes defined

- Max constant Time Error (cTE) contributed by a pluggable when host compensates for the "static" latency values of the module

Proposed additions to pluggables' Design Verification Tests (DVT)

- Tx and Rx propagation delays across a variety of corner conditions, generating histograms.
- "Static" values are the μ and "quasi-static" values are the 3σ of the distribution.
- Characterization is needed for each operating mode of the pluggable changing the propagation delay distribution (for instance: bit rates, number of FEC iterations, etc.)

New data needed in the pluggables' EEPROM

- The number of operation modes having different propagation delays
- "Static" and "quasi-static" propagation delay values for each operation mode
- informing the host what "current" operation mode is, and hence which set of values must be used

Ongoing collaborations

ITU-T SG15 Q13

- Liaison established!
- Open ongoing dialogue on the impact of pluggable optics on “node” and “link” level time synchronization accuracy

Entities with similar interests in “tight sync”

- Renown particle physics Institutions like CERN and Nikhef use pluggable optics for high-speed data transmission in their experiments.
- Accuracy of time synchronization is essential: sometimes telecom-grade is good enough, sometimes sub-femtosecond accuracy may be needed (for future-proofness).
- Very similar approach and significant subset of common use cases → we could join forces.

What may lie ahead for “tight sync”

SNIA/SFF , OIF/CMIS contributions for EEPROM

- Translating the high-level requirements in MOPA2.1 into a set of reserved EEPROM locations in the comprehensive maps maintained by these two standardization entities.

Contributing to the test and measurement discourse

- We identified “what” to measure, but “how” to measure it is also extremely important.
- This task is not in the MOPA scope. We will participate, but the discourse should take place in a different organization and involving different players (e.g. test equipment manufacturers).

Dynamic time error (dTE) characterization ?

- As long as 1:1 ratios between electrical lanes and optical lanes, cTE characterization is sufficient.
- On the road to 6G we may have to consider high-capacity optics with complex internal digital parts
- Depending on implementation details and internal clocking structure of those internal digital parts, also dTE could have to be considered.

twitter

LinkedIn